Open Questions in GaN Physics of Failure: *Focus on Channel Hot Carrier Stress*

NASA NEPP – June 2014

E. Heller*, B. Poling, A. Hilton**, J. Brown**, J. Beckman* and the HiREV Team**

***Air Force Research Laboratory**
****Wyle Laboratories**

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Outline

- **Motivation: HiREV mission**
- **Reminder: Survey of Open Literature**
- **Deltas in GaN Physics from Legacy Materials**

  → ***Enablers for new Physics of Failure***
- **Focus on Hot Electrons as a Failure Mode**
  - **Discussion of state of knowledge and ways forward**
- **Conclusions and Final Thoughts**

For this discussion:

- **Open literature and non-proprietary HiREV mat'l only**
- **Limited scope: materials to device level, no radiation effects**
- **<u>NOT</u> a final product with industry buy-in**

What is HiREV?
HiREV Mission and Vision:

HiREV = High **R**eliability **E**lectronics **V**irtual center

Mission

Ensure timely delivery of **independent, high-fidelity lifetime estimates** for electronic device technologies and their corresponding **underlying physics and chemistry of degradation and failure** to enable their qualification for critical DoD and US Space Programs.

Vision

A respected leader in lifetime assessment of electronic device technologies with a focus on **accelerating the insertion of emerging technologies** by developing **thorough understanding of their fundamental degradation and failure limits**.

Survey of Open Literature

Physics of Failure	Stressor	Failure Metric	Life Limiter
•Diffusion •Defect Percolation •TDDB at Gate •Surface barrier oxidation •Ohmic intermixing •Gate intermixing •**Critical elastic E** •**Cracking/pitting** •**Traps*** •Alloying, melting •Dislocations •SBH change •Interface Relax. •Multi-Fail models •**Unknown**	•**DC Electrical (I_D, V_D, V_G, V_{crit}, "semi-on")** •DC pulsed •RF •RF pulsed •**T_{BP} or T_{CH}** •Pulsed Temperature •UV light •Ambient gas •Ambient RF •Use of proxy parts •Starting conditions/ Processing marginality	•**DC electrical or parametric** •**RF electrical** •Model Guided •Transients •DLTS, DLOS, or I-DLTS •Other (PE/Thermal IR/noise/Raman/ SEM or AFM image judgment)	•T_{CH} "Negative" Ea Low Ea (0.12-0.39) **Mid Ea** Multiple Ea's, one part •**$V_{crit} = V_D - V_G$** •V_G •Hot electrons Which are… •Recoverable/not •Gradual/quick •Ambient Dominated •DC-RF similar/not •Unknown

Black = More Relevant for Hot Electrons

** Multi-dimensional space in Physics of Fill, E Depth, Type, Location, Physics of Fail*

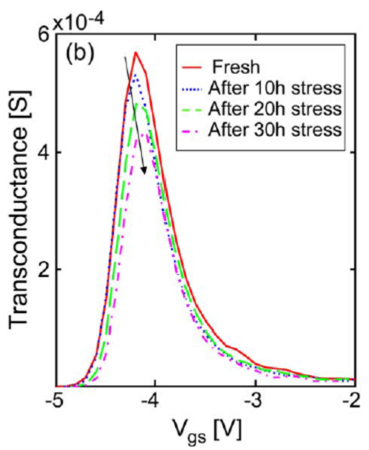
Physics of Failure (PoF) Enablers (approx. GaAs → GaN)

1. Ratio of Power Density (W/mm) to bulk thermal conductivity: ~2.5x
2. **Power Density (W/mm) and lots of hot carriers: ~10x**
3. Ratio of Power Density to Vol. Heat Capacity ~10x
4. **Evolving Materials & Processes**
5. GaN is grown on a non-native substrate
   a. **High Dislocation/Trap Density**
   b. Substrate Coeff. of Thermal Expansion (CTE) mismatch
6. Origin of 2DEG: Spontaneous polarization + PZ
7. **Wide bandgap ~2.5x; High critical breakdown field ~8x**

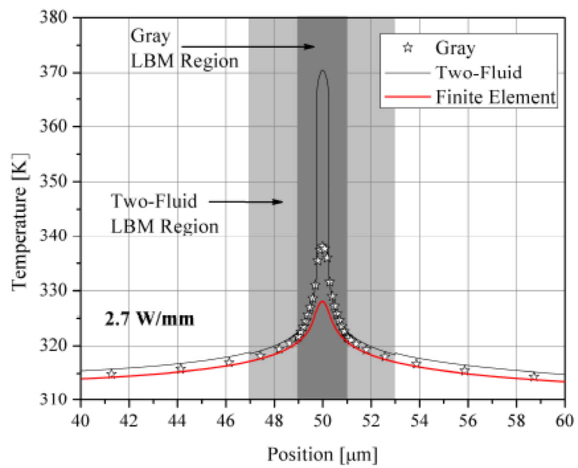
Physics of Failure (PoF) Enabler

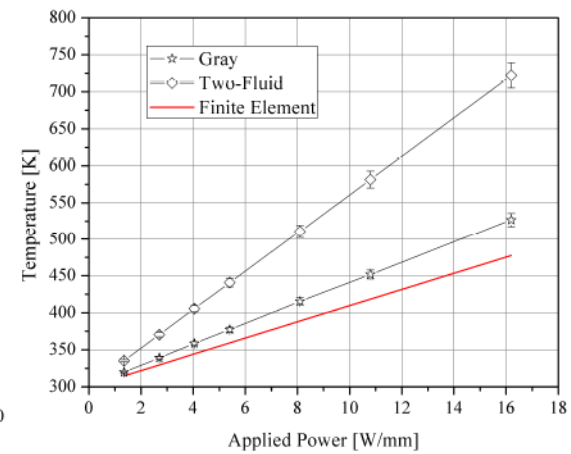
2. Power Density (W/mm) and lots of hot carriers:

- Example: About 10x greater W/mm for GaN vs GaAs.
- Concern: Open door for multi-electron, multi-phonon effects, more CHC stress.
- Resolution: *With application specific awareness and modern parts*, appears manageable.



Marco Silvestri, Michael J. Uren, and Martin Kuball, "Dynami Transconductance ispersion Characterization of Channel Hot-Carrier Stressed 0.25-μm AlGaN/GaN HEMTs", IEEE ELECTRON DEVICE LETTERS, VOL. 33, NO. 11, NOVEMBER 2012.





Christiansen, Adam. "Multiscale Modeling of Thermal Transport in Gallium Nitride Microelectronics." 2009. Doctoral Dissertation, Georgia Tech.

Possible Mitigation Options:

- **Test/Limit at Q point or max PE point as long as possible at high Vd. Back down Vd for application.**
- **Build in robustness to parametric shifts and/or perform burn-in.**

Physics of Failure (PoF) Enabler

4. Evolving Materials & Processes

Example: Diamond substrate → higher P density at same T_{CH}

- *But, this boosts hot electron density*

Example: Strained SiN[1] or diamond overlayer[2]

- *Mobility boost in Si increased CHC stress[3].*

[1] F. González-Posada Flores et al., The effects of processing of high-electron-mobility transistors on the strain state and the electrical properties of AlGaN/GaN structures, APPLIED PHYSICS LETTERS 95, 203504, 2009.
[2] B. Liu et al., NBTI Reliability of P-Channel Transistors With Diamond-Like Carbon Liner Having Ultrahigh Compressive Stress, IEEE ELECTRON DEVICE LETTERS, VOL. 30, NO. 8, Aug. 2009, pp. 867-869.
[3] J. Martin-Martinez et al., "Aging mechanisms in strained Si/high-k based pMOS transistors. Implications in CMOS circuits", 2011 Spanish Conference on Electron Devices (CDE), 8-11 Feb. 2011, pp1-4.

Possible Mitigation Options:

- **Fortunately, GaN HEMTs appear robust.**
- **Apply caution to enhancements meant to boost carrier mobility.**
- **Beware performance boosting tricks, or the sudden appearance or change in *processing conditions* of overlayer.**
- **Test/Limit extreme abs(Vd – Vg) bias at extremes of ambient temperatures, especially at low T.**

PoF-E: Novel physics

5a. GaN is grown on a non-native substrate:

- About 10^9 dislocations cm^{-2}
- Concern: Opens doors for low E_a diffusion, **lower E_a defect creation pathways,** thermal boundary resistance (TBR), coefficient of thermal expansion (CTE) mismatch and process stresses.
- **Fortunately, mitigation strategies exist, this appear to be a non-issue**

5b. Channel is *not* dopant created!

- Intrinsic Spontaneous and *Piezoelectric* Charge.
- Strong incentive to maximize tensile stress in AlGaN
- Can be boosted by dopant.

Possible Mitigation Options:

- **Fortunately, GaN HEMTs appear robust.**
- **Very long tests, measure or assume worst case TBR, thermal+power cycling, proper ambient (water vapor, etc.).**
- **Raman for GaN mechanical stress before/after electrical stress.**

PoF-E: Bandgap

7a. Wide Bandgap (eV):

- Example: About 2.5x for GaN vs GaAs.
- Very hot electron effects, holes supply a lot of energy,
- Semi-infinite trap lifetimes, especially when cold.
- Workhorse tool DLTS will not measure the deeper traps at room T.
- Concern: Deeper traps, and semi-infinite thermal resets.
- Resolution: *Application specific awareness*.

Possible Mitigation Options:

- De-rate for Vd. Fortunately technology has a lot a margin to de-rate.
- Yet, high Vd can reset traps & mask an issue! Verify system operates cold and at lowest allowed Vd operation.
- Verify low & high T operation *in the dark*, especially circuit corners in Vt, near Vt device operation, *low Vd* operation, and *low Vd* operation just after the coldest, most extreme *high Vd* at hard pinch-off for in-use.

PoF-E: Breakdown Field

7b. High critical breakdown field (V/cm):

- **Example: About 8x greater for GaN vs GaAs.**
- **Concerns: Very high E fields, very hot electron effects, *not* accelerated thermally, drift by E field of charged traps, high inverse PZ mech. stresses!**
- **Channel noise, Ig noise, and Ig leakage changes.**
- **Resolution: GaN is tough! With awareness, may not be an issue.**

Possible Mitigation Options:

- **Can de-rate for Vd. Technology has a lot a margin to de-rate by. Select for lowest Ig leakage parts.**
- **High Vd, high Abs(Vd-Vg) can supply energy to fail modes. Test high Abs(Vd-Vg) at low/high T.**
- **Select lowest Ig parts. Might use low/high Ig as an ALT “stressor”, with increase in Ig, Ig noise as fail metric.**
- **Watch for cratering (esp. on test)! High Vd means that system capacitances can feed energy as Vd^2!**
- ***Not expected to be an issue for RF devices at nominal Q point.***

CHC stress: Background

CHC in Si at-a-glance:

1. Physics of Failure:

- Cited as a free electron with $E - E_C > 2$ eV to break Si-H bond at interface[1], or ~3.2 eV to enter SiO_2 (Si/SiO_2 interface barrier).

2. Scaling Seen/Expected:

- Ln(Deg rate) scales with $1/V_D$ for a given device[2, 3],

  This is closely related to Ln(Impact Ionization rate) which scales with $1/E_{PEAK}$ (Chynoweth's law[4])

- Power law time dependence as set conditions typical with slowdown over time[3], cited as charge buildup slowing kinetics of future events[1].

3. Parametric data affected and fail metrics:

- V_{th}, G_m, and/or pinch-off characteristics at the drain corner of the gate affected[2, 5, 6].

- Example fail metrics: V_{th} shift of 10 mV, 10% drop in I_D[5] or V_{th} shift of 50 mV, 10% drop in I_D[7]

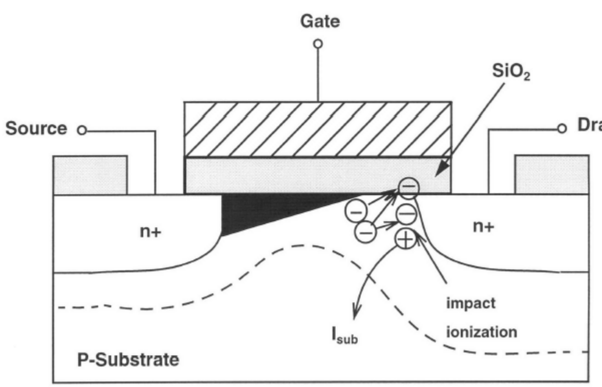
4. Proxies for degradation:

- Can track substrate current[2] or substrate to I_D ratio (n channel)[3] or gate current (p channel)[2, 7] as proxies for degradation (both measuring flux greater than a cutoff E).

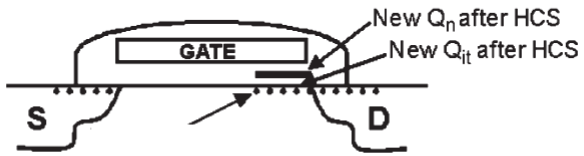
1. *Sentaurus Device User Manual*, Ver. E-2010.12, Synopsys, Inc., Mountain View, CA, Dec. 2010
2. http://www.cacs.louisiana.edu/labs/vlsi_old/secure/presentations/FALL05/abhijit-hot-carrier-effect.ppt
3. JEDEC JESD28-1 and JEDEC JESD28A
4. A. G. Chynoweth, "Ionization Rates for Electrons and Holes in Silicon," *Physical Review*, Vol. 109, No. 5, pp. 1537–1540, 1958.
5. Wenjie Wang, "Hot-Carrier Reliability Assessment in CMOS Digital Integrated Circuits", Ph. D. Dissertation, Massachusetts Institute of Technology, 1998.
6. Tang et al., "Hot-Carrier and Fowler–Nordheim (FN) Tunneling Stresses on RF Reliability of 40-nm PMOSFETs With and Without SiGe Source/Drain", IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 56, NO. 4, APRIL 2009, pp. 678-682
7. JEDEC JESD60A

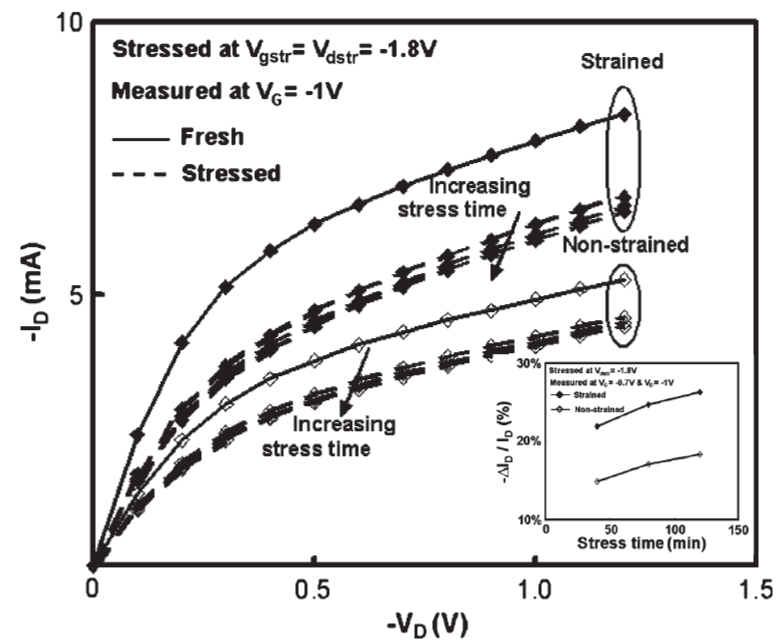
CHC stress: Background

CHC in Si, continued



Wenjie Wang, "Hot-Carrier Reliability Assessment in CMOS Digital Integrated Circuits", Ph. D. Dissertation, Massachusetts Institute of Technology, 1998.





Tang et al., "Hot-Carrier and Fowler–Nordheim (FN) Tunneling Stresses on RF Reliability of 40-nm PMOSFETs With and Without SiGe Source/Drain", IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 56, NO. 4, APRIL 2009, pp. 678-682.

CHC stress: Background

CHC in GaN HEMTs at-a-glance:

1. Physics of Failure:

- Cited as a free electron with $E - E_C > 2.1$ eV to break H bond to substitutional O in AlGaN[1]. Higher energy degradation modes expected too[1]. Defect creation energy can be a strong function of things like the Fermi level position with respect to the bands[6, 7]

2. Scaling Seen/Expected:

- Ln(Photon Emission/I_D) scales with $1/(V_D - V_{DSat})$ for a given device[2, 3],
  This is closely related to Si, where Ln(Impact Ionization rate) which scales with $1/E_{PEAK}$ (Chynoweth's law[4])
- Time to Failure and Photon Emission power low seen (1/TTF proportional to light^1.4)[5].
- GaN may[8] or may not have power law time dependence (slow down) seen in Si[5].

3. Parametric data affected:

- R_{on}[5], ~50mV V_{th}[1], ~20% G_m drop at 10V[1] or 20V[2], ~20% I_{dss} drop at 30V[8], and/or gate lag characteristics[2]

4. Proxies for degradation:

- Can track photon emission! But source FP devices are *almost dark*. Anything else???

1. S. Mukherjee, Y. Puzyrev, J. Chen, R. D. Schrimpf, D. M. Fleetwood, and S. T. Pantelides, "Modeling hot-carrier-induced degradation in AlGaN/GaN HEMTs," Reliability of Compound Semiconductors Workshop, New Orleans, LA, May 13, 2013.
2. G. Meneghesso, G. Verzellesi, F. Danesin, F. Rampazzo, F. Zanon, A. Tazzoli, M. Meneghini, and E. Zanoni, "Reliability of GaN High-Electron-Mobility Transistors: State of the Art and Perspectives" *IEEE Transactions on Device and Materials Reliability*, Vol. 8, No. 2, pp. 332-343, June 2008.
3. M. Meneghini et al., "Impact of Hot Electrons on the Reliability of AlGaN/GaN High Electron Mobility Transistors", *Proc. IEEE Int. Rel. Phys. Symp. (IRPS)*, 2012.
4. A. G. Chynoweth, "Ionization Rates for Electrons and Holes in Silicon," *Physical Review*, Vol. 109, No. 5, pp. 1537–1540, 1958.
5. G. Meneghesso et al., Degradation of AlGaN/GaN HEMT devices: Role of reverse-bias and hot electron stress, Microelectronic Engineering 109 (2013) 257–261.
6. Y. S. Puzyrev, T. Roy, M. Beck, B. R. Tuttle, R. D. Schrimpf, D. M. Fleetwood, and S. T. Pantelides "Dehydrogenation of defects and hot-electron degradation in GaN high-electron-mobility transistors", *Journal of Applied Physics,* Vol. 109, 034501, 2011.
7. Y. S. Puzyrev, B. R. Tuttle, R. D. Schrimpf, D. M. Fleetwood, and S. T. Pantelides, "Theory of hot-carrier-induced phenomena in GaN high-electron-mobility transistors", *Appl. Phys. Lett.* Vol. 96, 053505, 2010.
8. M. Meneghini et al., "Degradation of AlGaN/GaN high electron mobility transistors related to hot electrons", Appl. Phys. Lett. 100, 233508 (2012)

A Main Open Lit Reported Fail Mode: Channel Hot Carrier (CHC) Stress

Others' observations on CHC Stress…

- Worst at high E field near pinch-off with some electrons
- NOT the highest power point.
- NOT very thermally accelerated if at all!
- A knowable test methodology.
  - Run as highest Vd near Q point or peak PE point.
- Concern: Peak stress point is how we want to run an RF device!
- Concern: Vd extrapolation feasible but might be an issue!
  - Is FP effect on 2DEG depletion the same at operating condition as ALT???

Possible Mitigation Options:
- Minimize extrapolation to mission life (test as long as possible)
- Test at highest mission Vd at or near Q point and/or at or near highest PE point.
- Minimize Vd, track t=0 Idss, select for application accordingly.

Light emission (PE) and CHC stress

PE approximately tracks degradation rate

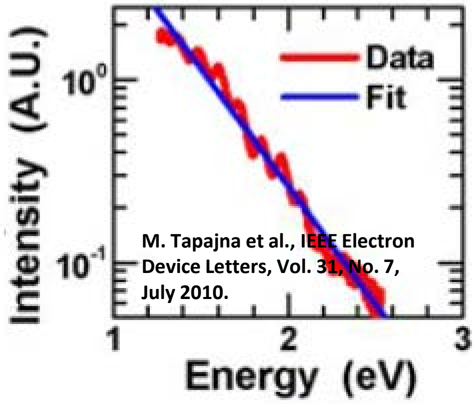
For a set device size (periphery), set drain bias at least...

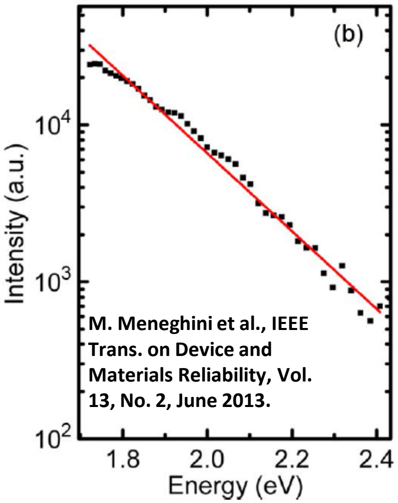
PE reasonable fit to Chynoweth's law (based on impact ionization)

But PE usually measured for E > 1.1 eV while E_g = 3.4 eV!

PE supports Boltzmann electron temperature approximation

Probably not the whole story! High E tail?





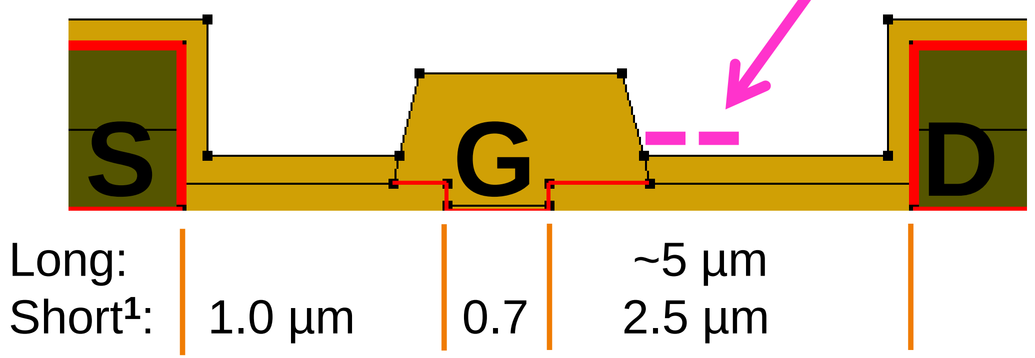
HiREV Observations - Modeling

Shifting gears a little…

From reporting open literature to early HiREV results.

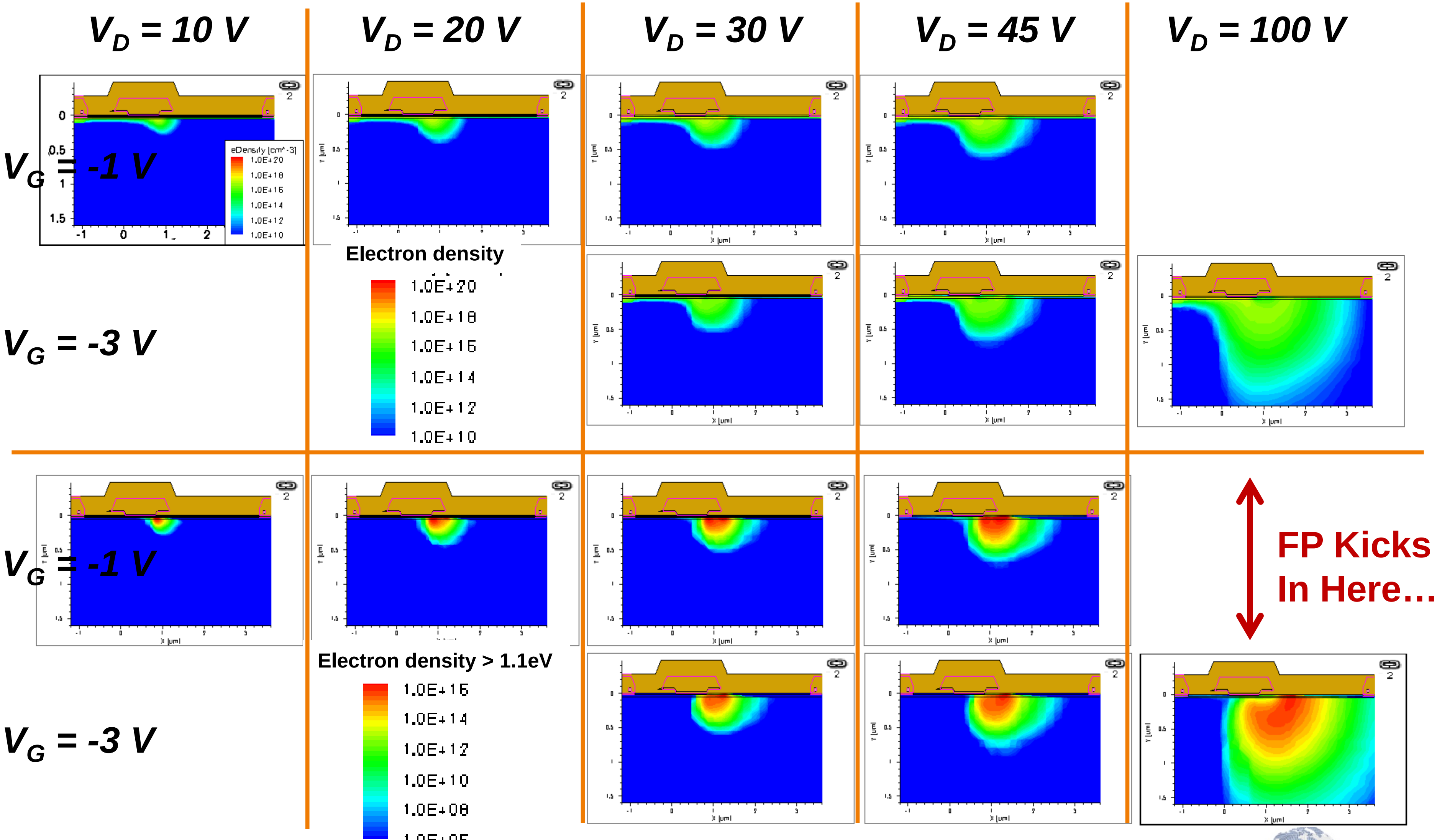
Optional Source Connected Field Plate (FP)

Model layout:



[1] M. Tapajna et al., IEEE Electron Device Letters, Vol. 31, No. 7, July 2010.

HiREV Observations - Modeling



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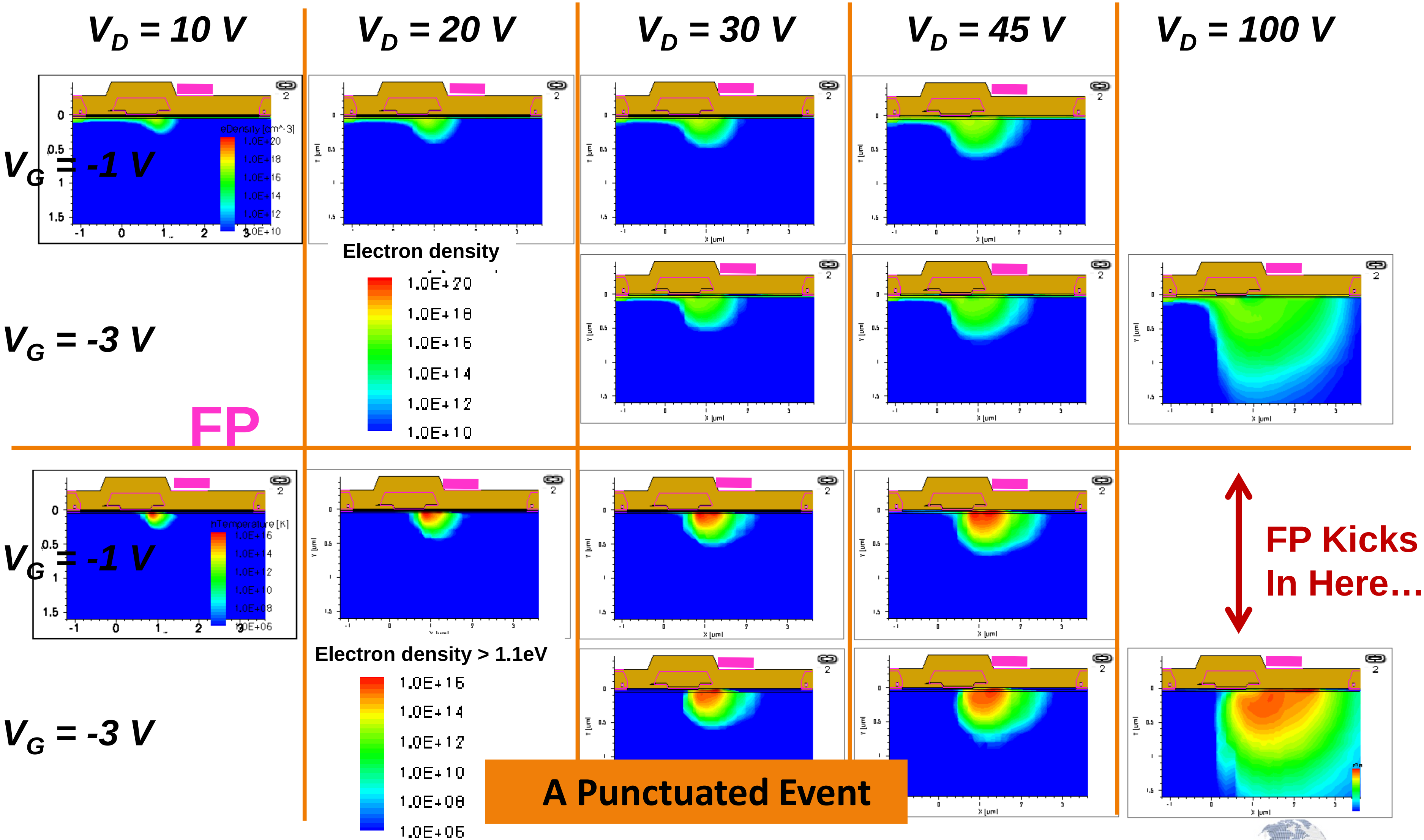
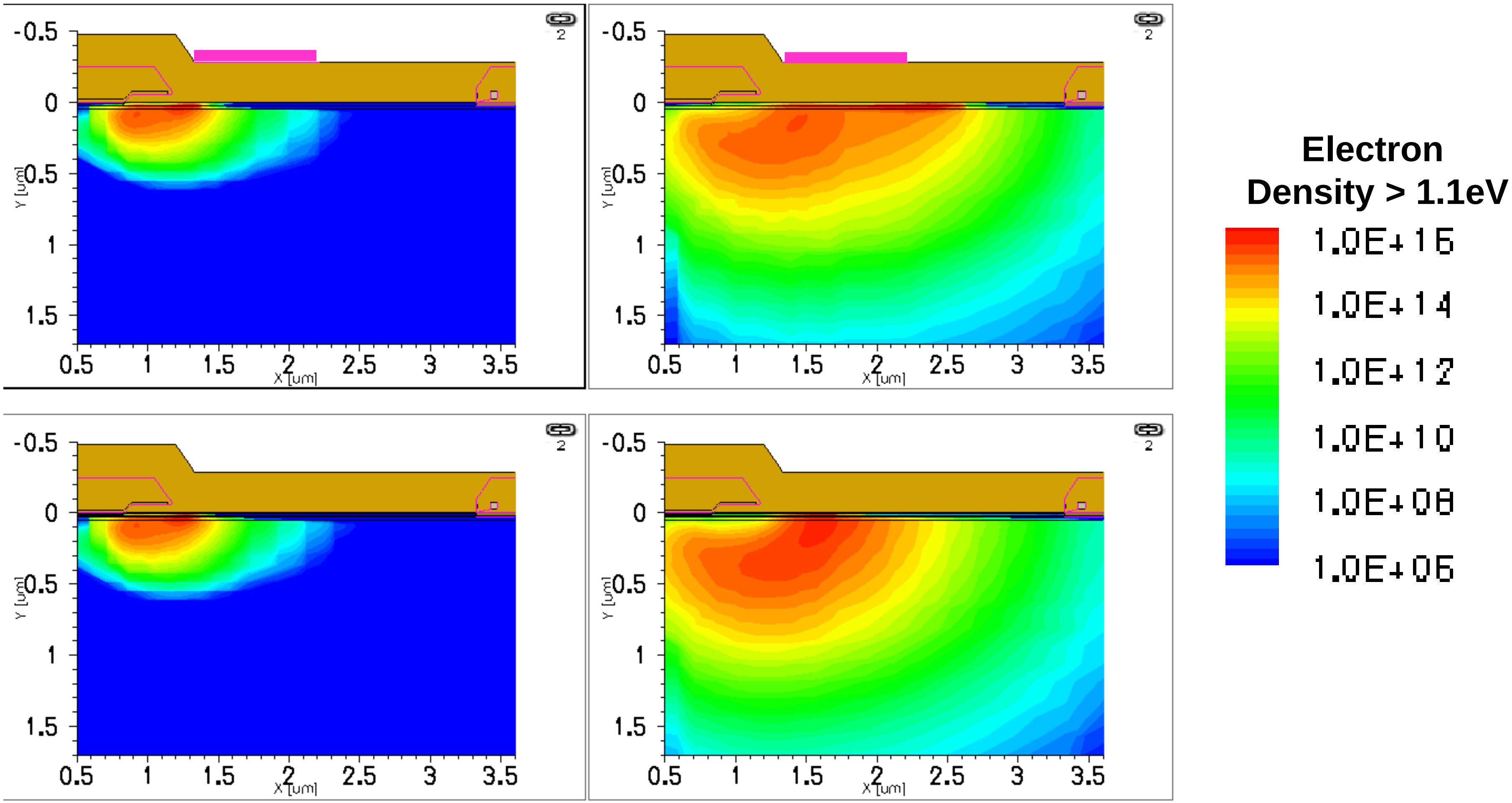
HiREV Observations - Modeling

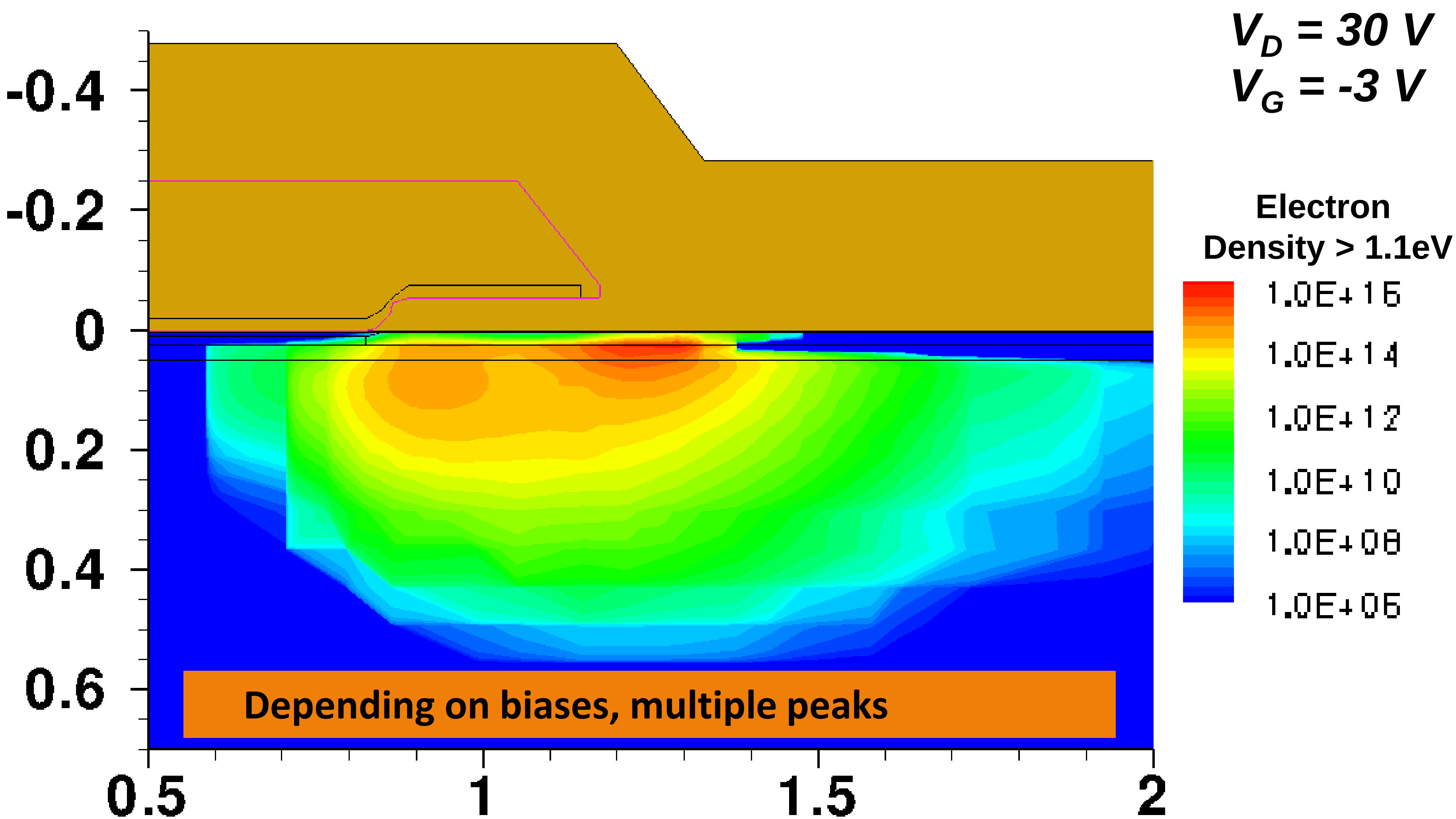


HiREV Observations - Modeling

$V_D = 30\ V, V_G = -3\ V$ $V_D = 100\ V, V_G = -3\ V$



HiREV Observations - Modeling

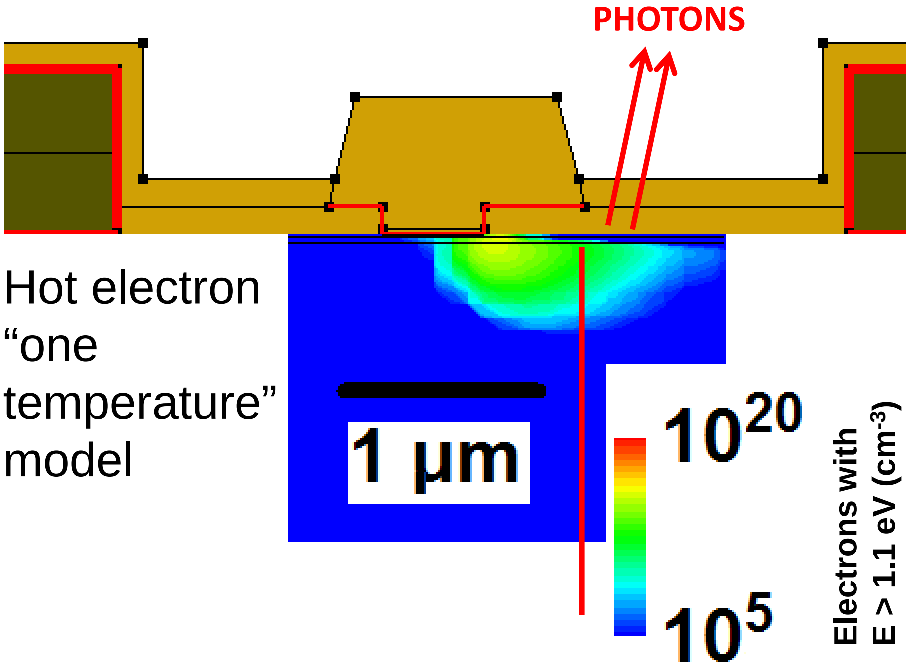


HiREV Observations - Modeling

Thoughts on Light emission (PE) as CHC proxy

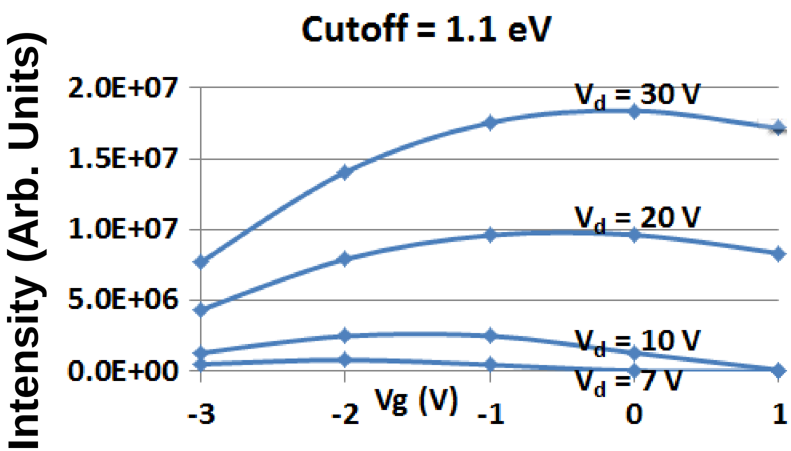
- **Vast majority of light predicted *under the gate***

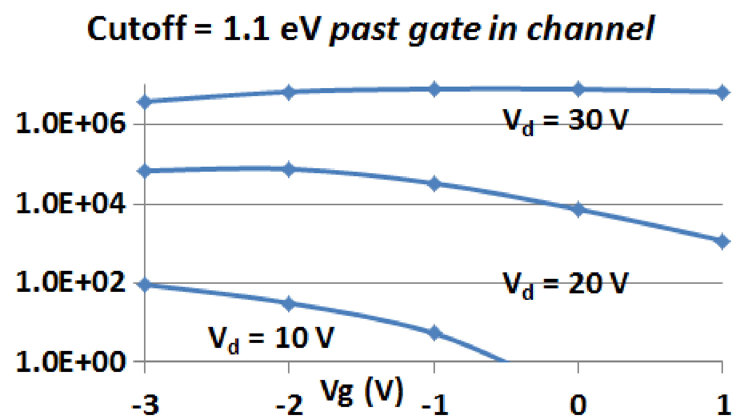
Hot electron "one temperature" model

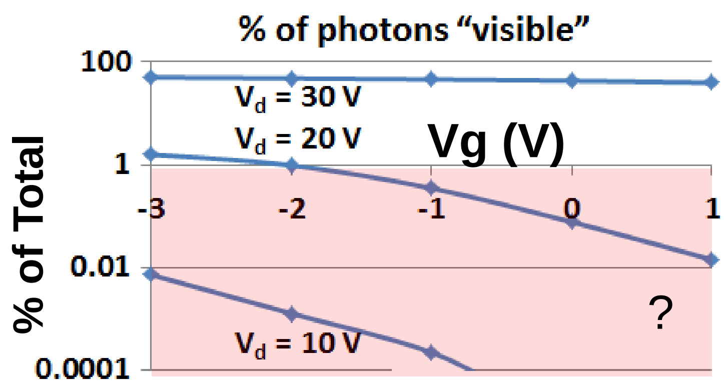


What does this mean for topside PE characterization???

Thoughts on Light emission (PE)



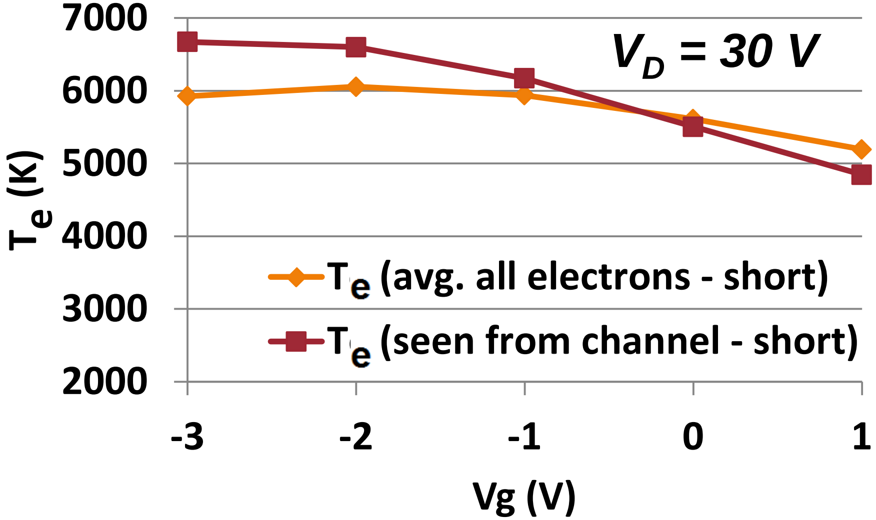


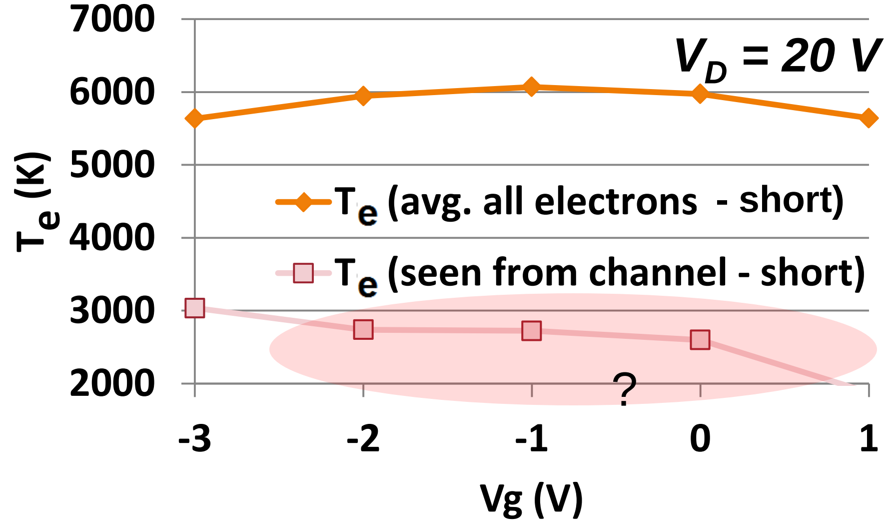


Probably not seeing most of the action, especially for a low Vd/big FP!

HiREV Observations - Modeling

Thoughts on Light emission (PE)



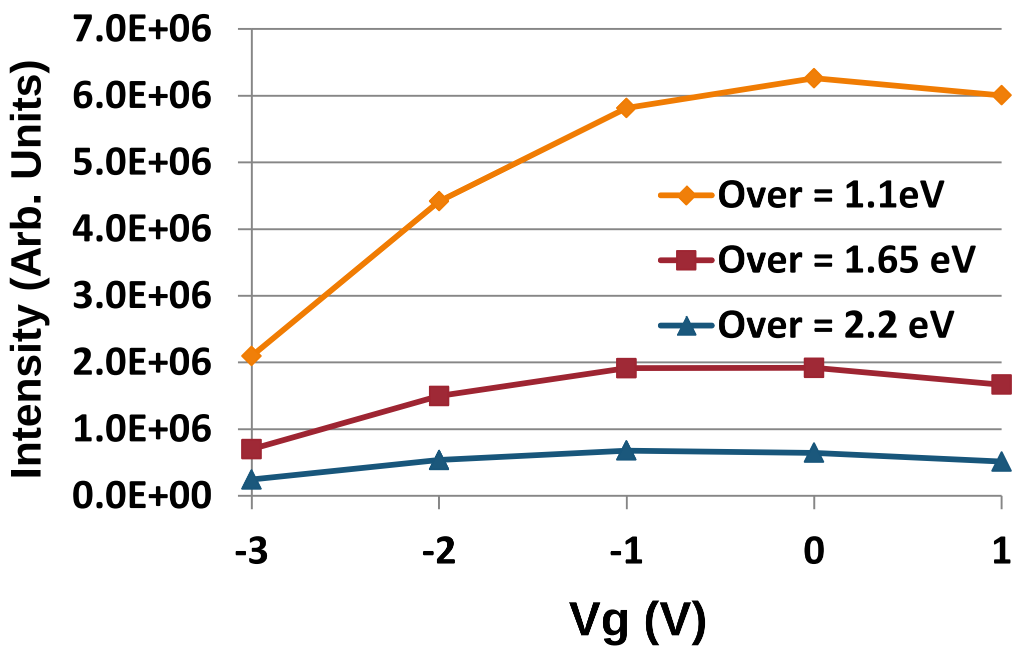


M-B fit for E > 1.1 eV
"short channel"

30V: Slightly skewed picture – depends on what light is visible.
20V: Only the extreme tail makes it past the gate!

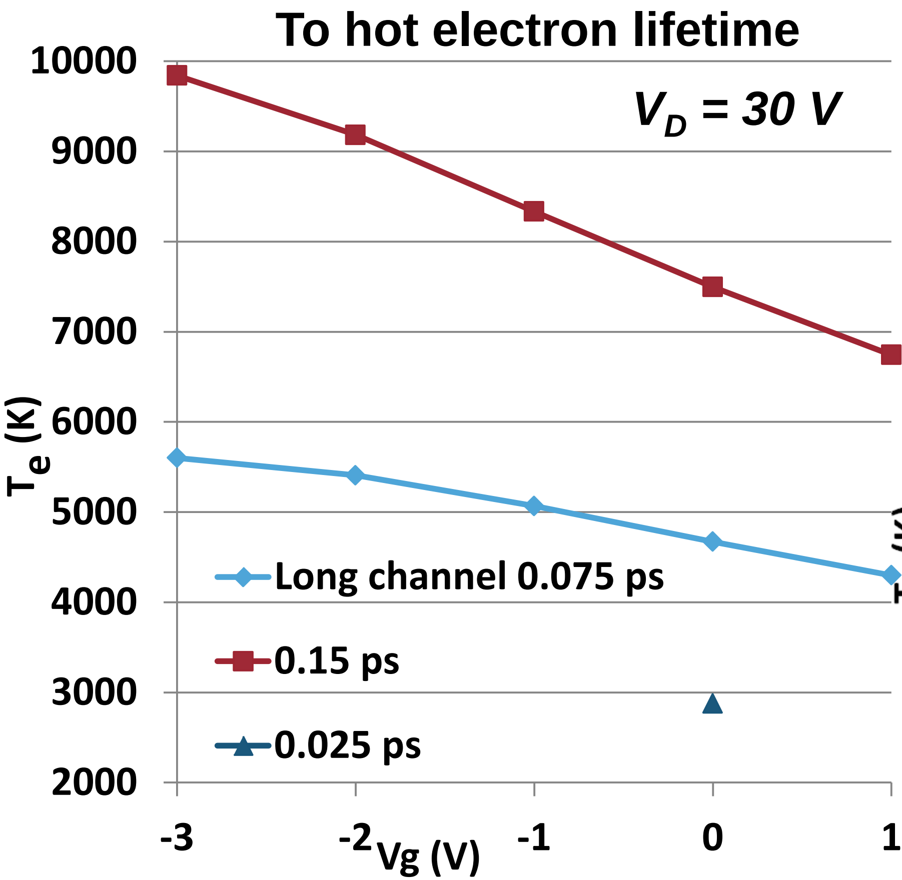
HiREV Observations - Modeling

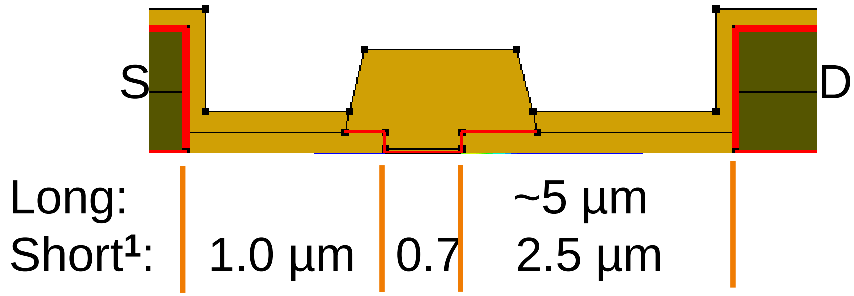
Thoughts on Cutoff Energy for Light Emission (PE)



HiREV Observations - Modeling

Model input sensitivity…





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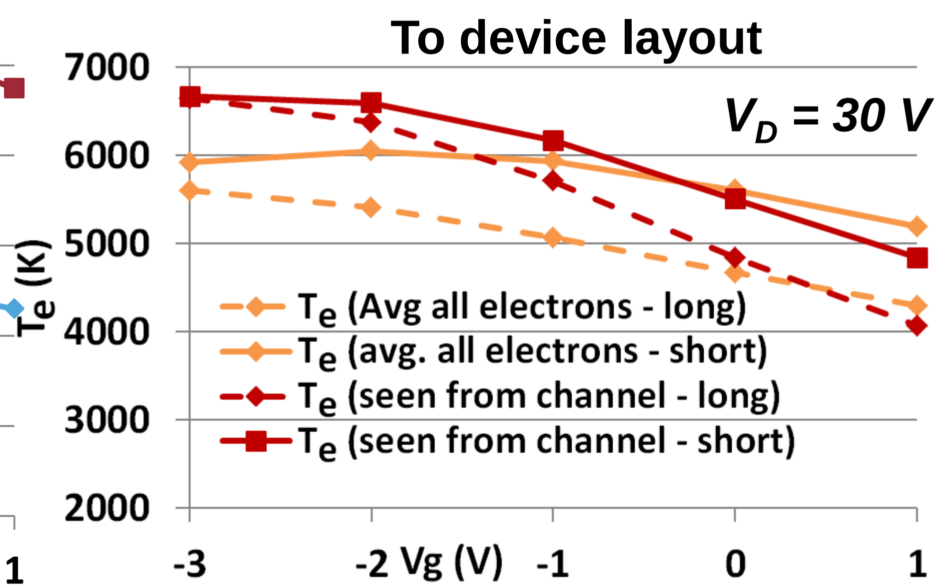
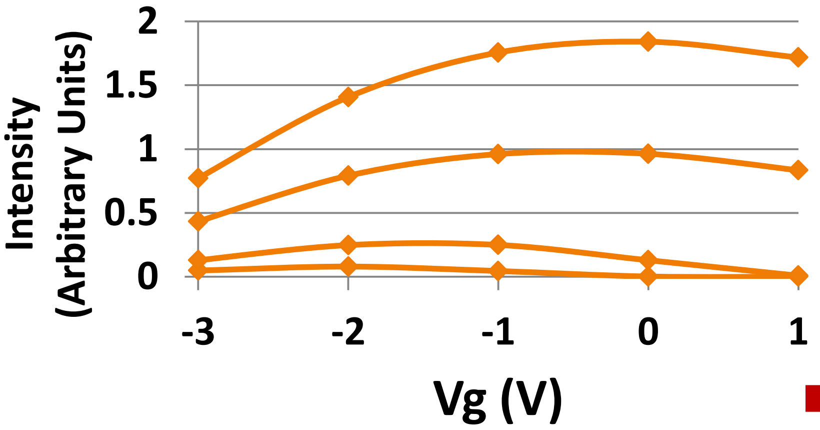
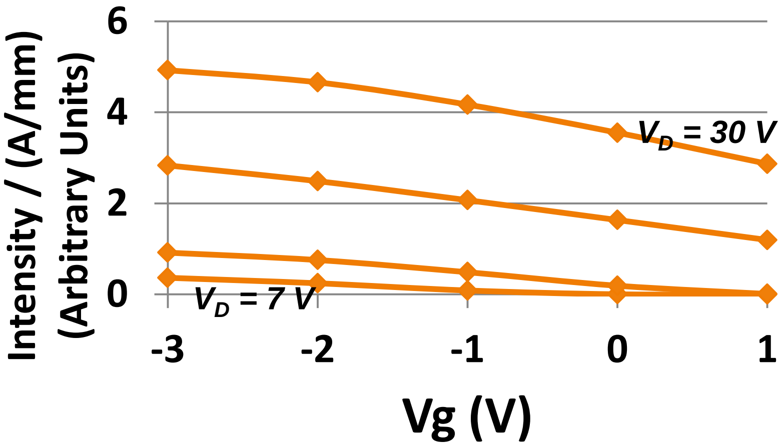
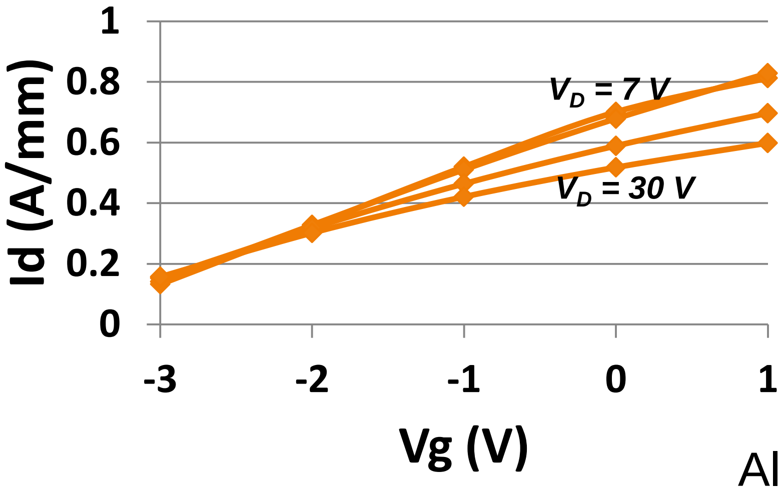


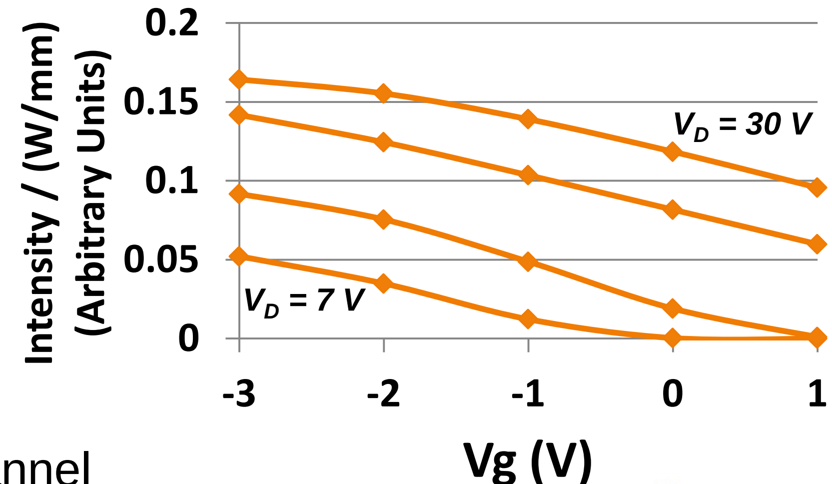
HiREV Observations - Modeling

A word on Fail Metrics and design space:









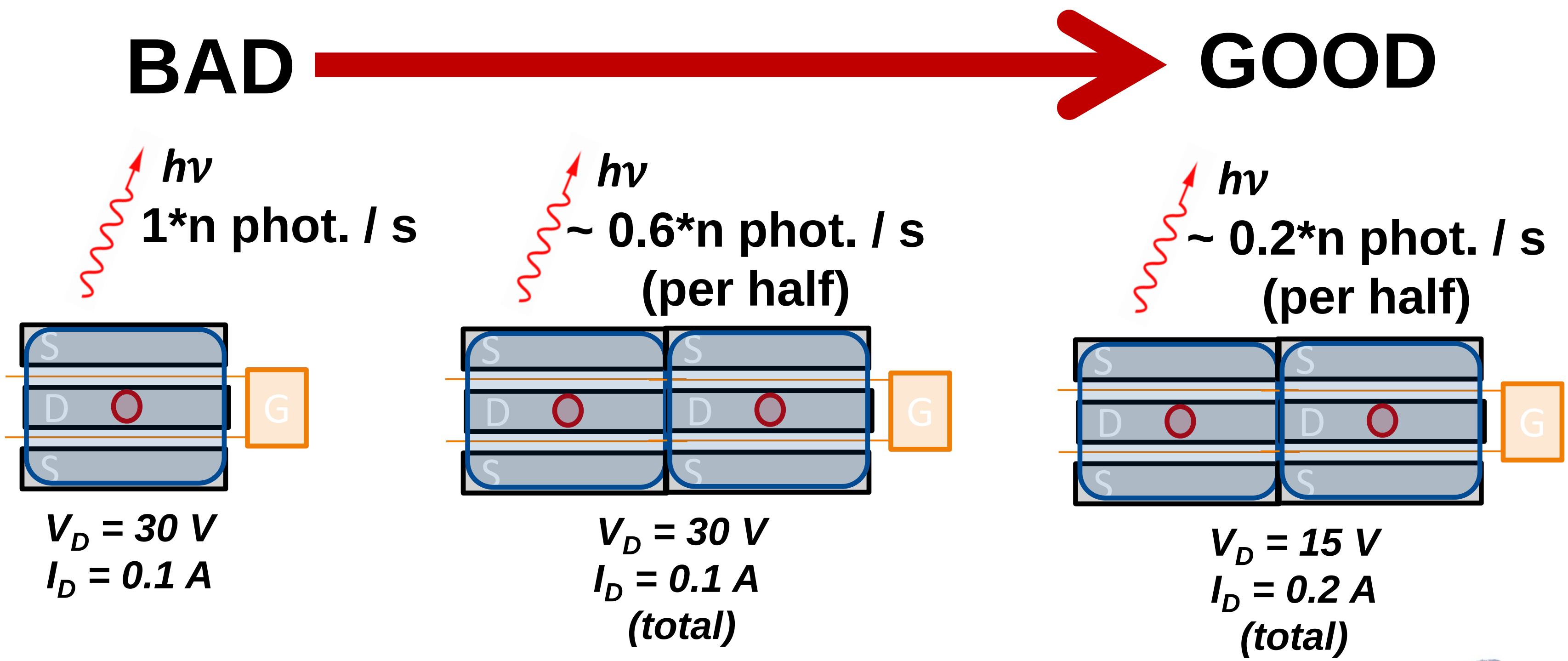
All long channel

HiREV Observations - Modeling

A word on Fail Metrics and design space:

Assume Intensity ∝ Degradation rate.

For a set device size and drain bias at least…



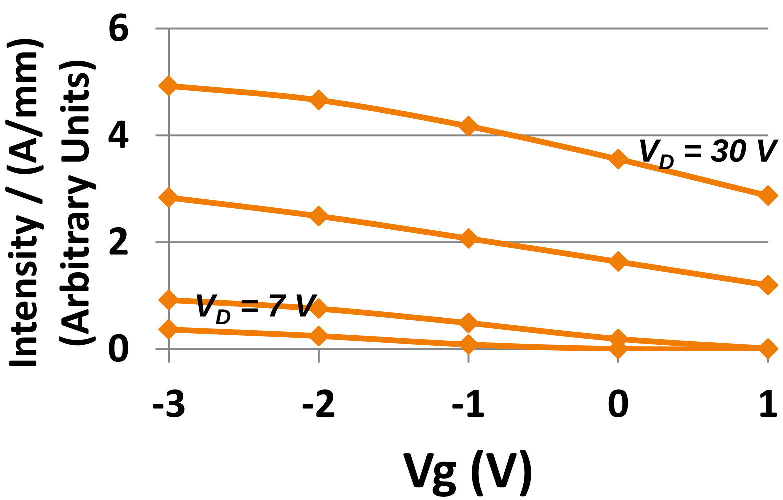
HiREV Observations - Experiment

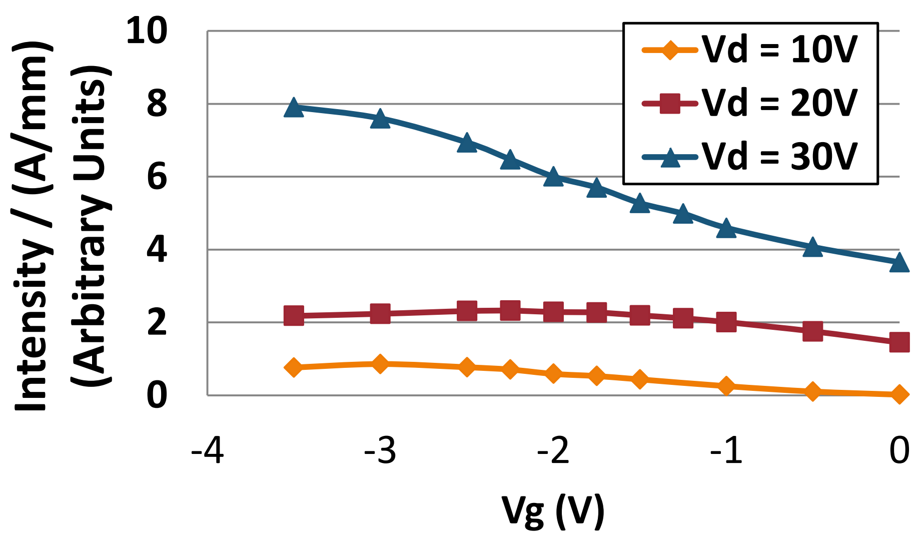
HiREV observations on *total device* light (photons/s)

- Multiple devices (no SCFP)

- Insensitive to test sequence, camera focus, etc.

- Slight ***drop*** with increasing baseplate temperature



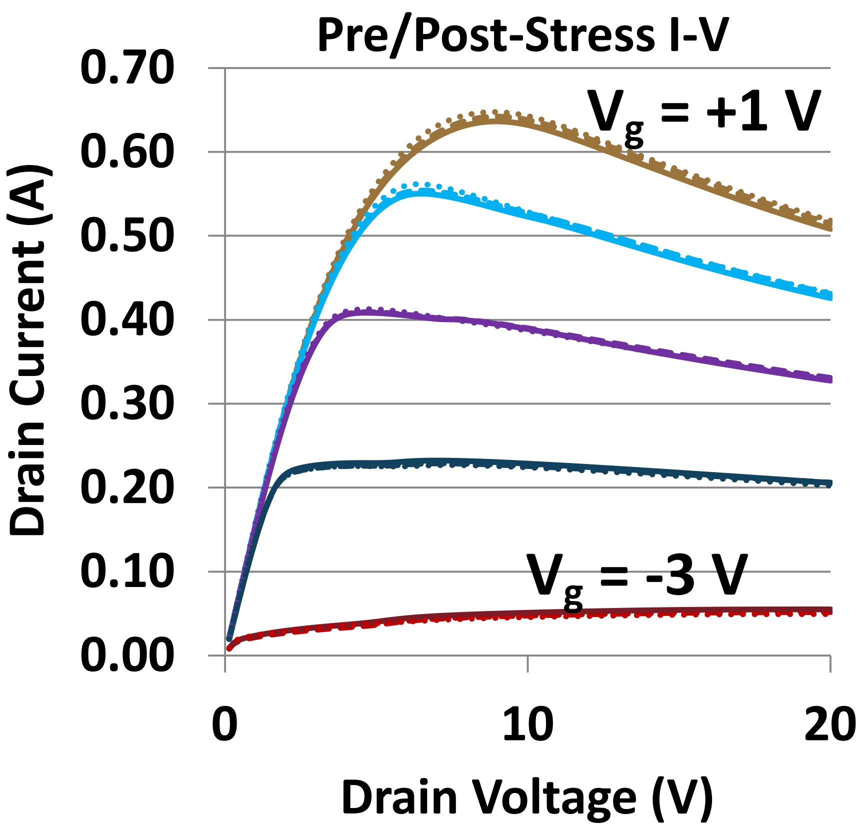


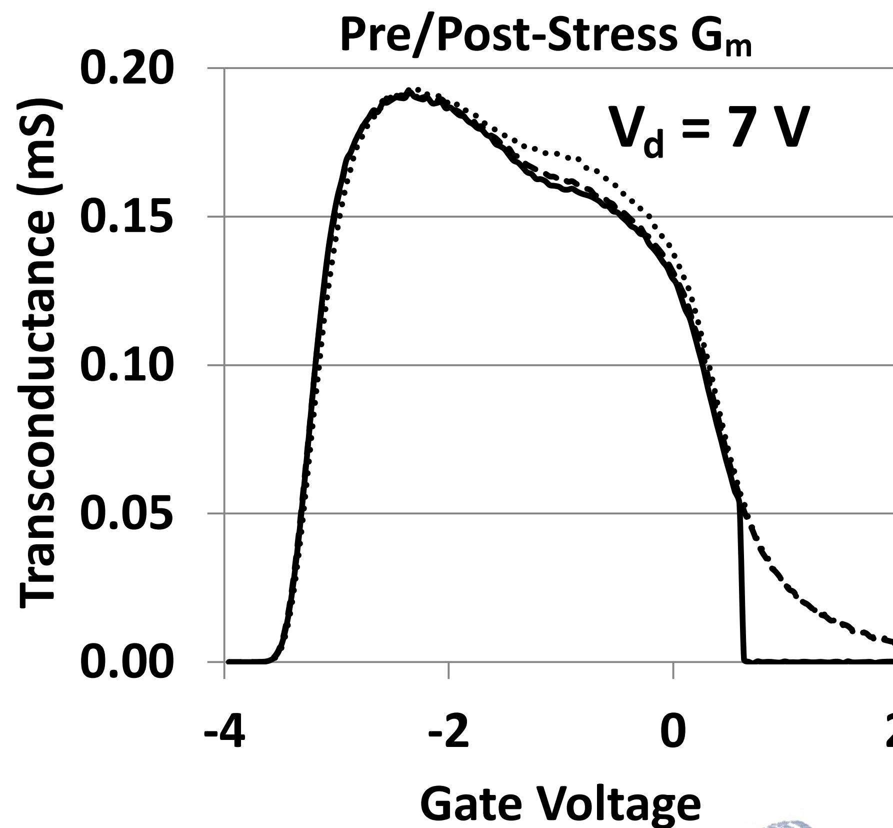
Qualitative agreement with modeling of entire emission, not channel only emission!

HiREV Observations - Experiment

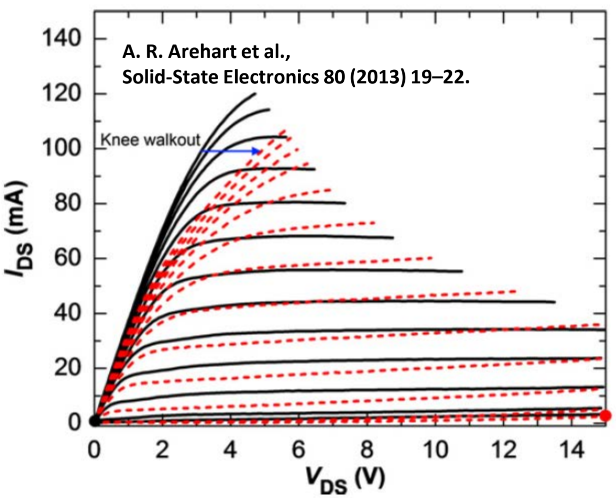
- Subtle ***increase*** in G_m
  (open lit shows G_m drop)

Pre Stress
Post 210 h @ 20V
Post 70 h @ **90V (~18V/um)**

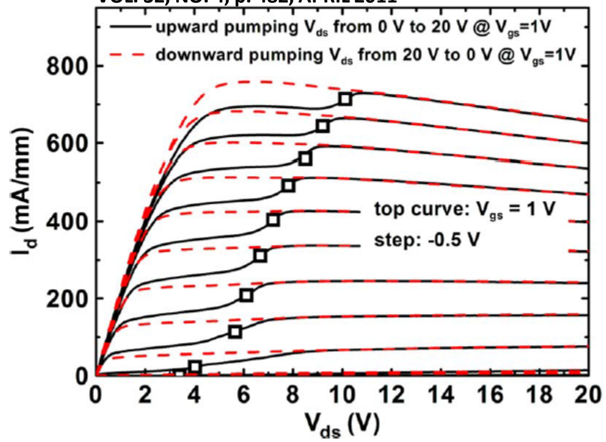




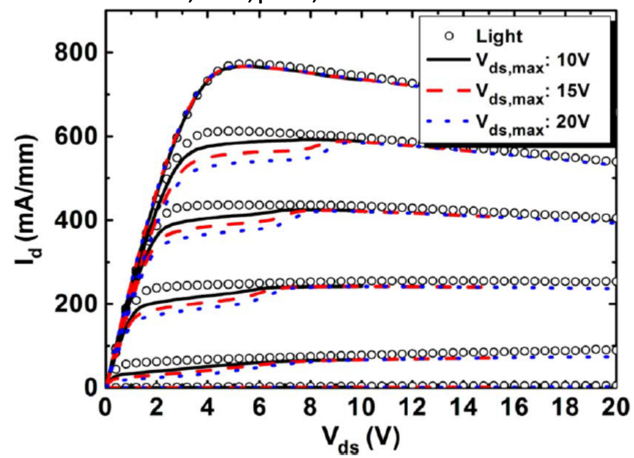
Kinks, traps, etc.



M. Wang and K. J. Chen, IEEE Electron Device Letters, VOL. 32, NO. 4, p. 482, APRIL 2011



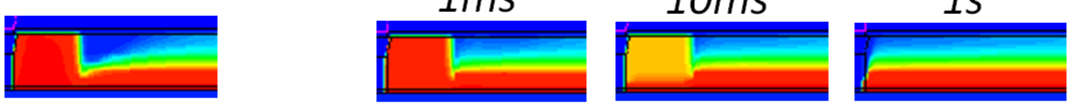
M. Wang and K. J. Chen, IEEE Electron Device Letters, VOL. 32, NO. 4, p. 482, APRIL 2011



V_G=-3.5V and V_D=15V $\qquad$ V_G=0V and V_D=0.35V

Trapped charge recovery

1ms $\qquad$ 10ms $\qquad$ 1s



Fill $\qquad$ HiREV $\qquad$ Emptying

Possible Mitigation Options:

- **Expect *repeatable* shifts in some parametrics; Ron, Idss, etc. Large device-device variation; select for best parts.**
- **Design flexibility for these into circuit. Test low & high T operation extremes and in-use bias sequences/lighting!**
- **Expect slightly worse trapping behavior post-stress.**
- **Beware process changes increasing dislocation density or changing epi stack.**

Kinks, traps, etc.

HiREV observations (Electrical test)

- Many effects (Kinks, trapping, set with bias and reset with light, time, etc.)
    - Need to understand what changes are temporary and what are permanent.
    - Need for a well thought out test procedure so you are measuring what you want to measure and not a mixture of effects.
    - Measure multiple parameters to separate one effect from another

Conclusions and Final Thoughts

CHC Path Forward:

- **Understand Physics of failure (PoF)!**
  - Hypothesis: ~2eV electrons de-passivate existing defects
  - Hypothesis: NOT impact ionization (recall E_g = 3.4 eV)
  - Chynoweth's law valid? Default to $E_{CHC} = (V_D - V_S)/L_{GD}$?
  - If latter, reported E_{CHC} ~ 6, 7, 15 V/µm; degradation in ~10's h. *Contrast with E_{BR}* ~ 300 V/µm and our success at 18 V/µm.
- **Common language required but lacking!**
  - Are parts tested dated or modern, low or high volume?
  - Are failures Intrinsic? Extrinsic?
  - Not enough information in publications for PoF!

Need *full* documentation of channel dimensions

Reminder: One Piece

- Many Deltas in Physics from Legacy Materials
  - Most relate to fact that GaN can be pushed harder than prior materials.
  - Some are intrinsic to the new materials system.
- *Understand your application!*
- Literature has found a few main mechanisms.
  - Classic thermal "3T ALT" wear-out. The one you were warned about!
  - **Channel Hot Carrier (CHC) stress**
  - High Voltage "critical field" failures.
- Traps can be thought of as a fourth failure mode but many characteristics differ from other modes.

SUPPLEMENTAL

Switching Gears

- We want a well defined Physics of Failure, Stressor(s), Fail Metric(s)
  (like Si CMOS)

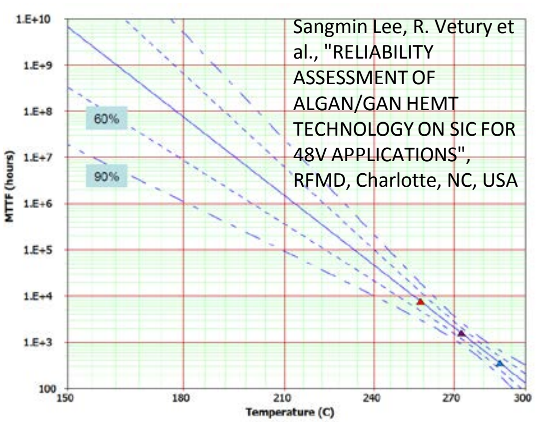
  → Well defined "path" to follow for reliable conclusions

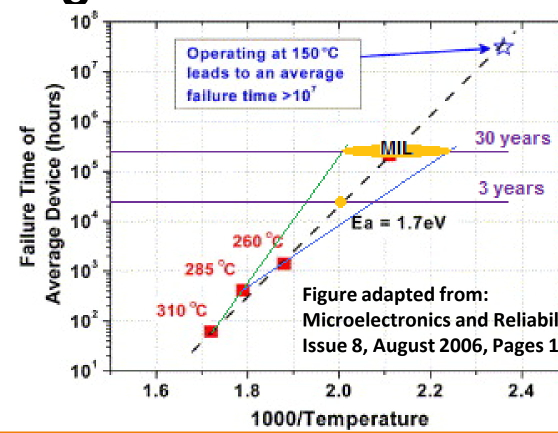
This time its…
Col. Mustard,
In the Study,
Lead pipe.

Main Open Lit Reported Fail Modes

1. Thermal (3T ALT)

- "The standard model"
- Recipe: Boost T_{bp}, maintain everything else as well as possible
- A known test methodology, works for a known fail mode.
- Concern: Tests *one stressor*. T is at *fail site*, yet even if that is known T still varies 10's of K over a large device.





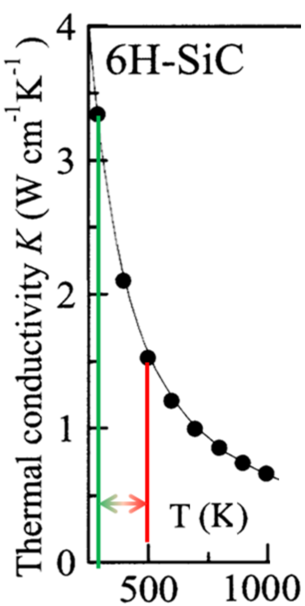
Possible Mitigation Options:

- Minimize extrapolation to mission life (test as long as possible). Leave parts on test if you can.
- Understand error bars in lifetimes of data points *and Ea*.
- Verify lowest plausible Ea will not be an issue!

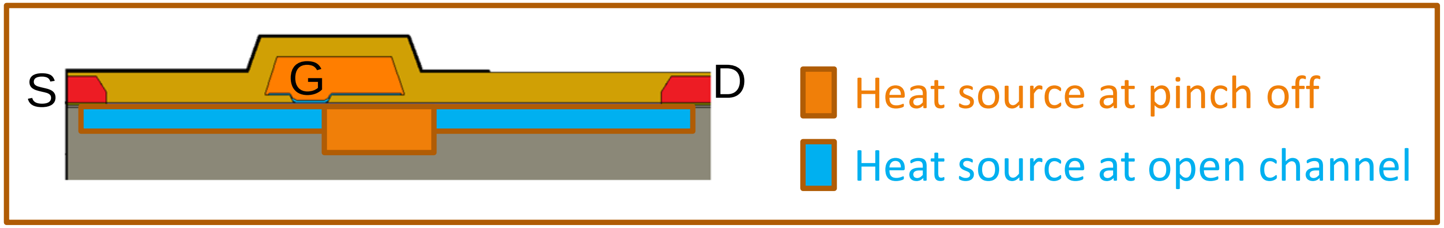
Physics of Failure (PoF) Enabler

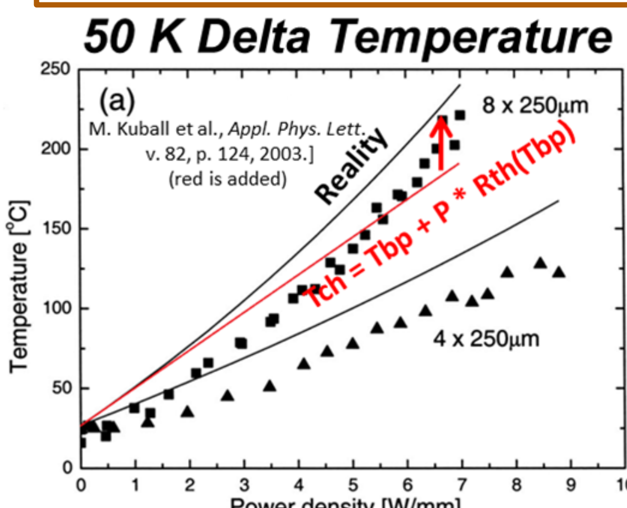
1. Ratio of Power Density (W/mm) to bulk thermal conductivity (W/m/K):

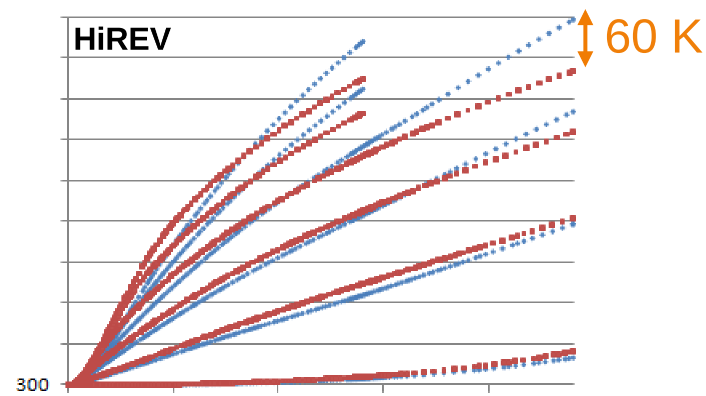
- Example: About 2.5x greater for GaN vs GaAs.
- Concern: Nonlinear effects increase vs. “legacy” power density.
- Resolution: A clear path for modest de-rating exists.



OFF ON
200 K







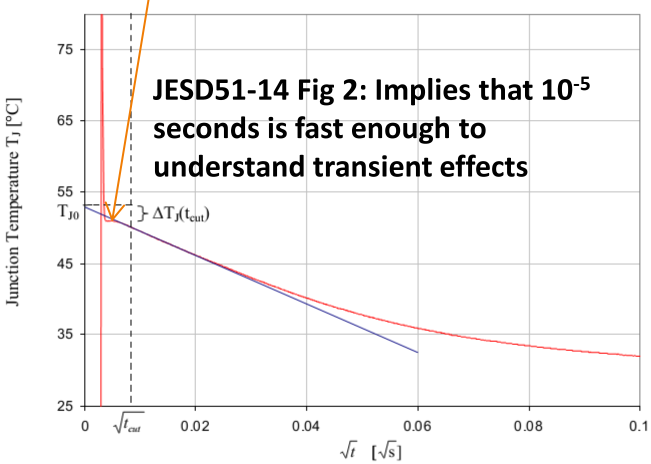
- Modeled “True” Peak Temperature
- $T_{ch} = T_{bp}$ + fn(P, Tbp) – Std. Spec Sheet T

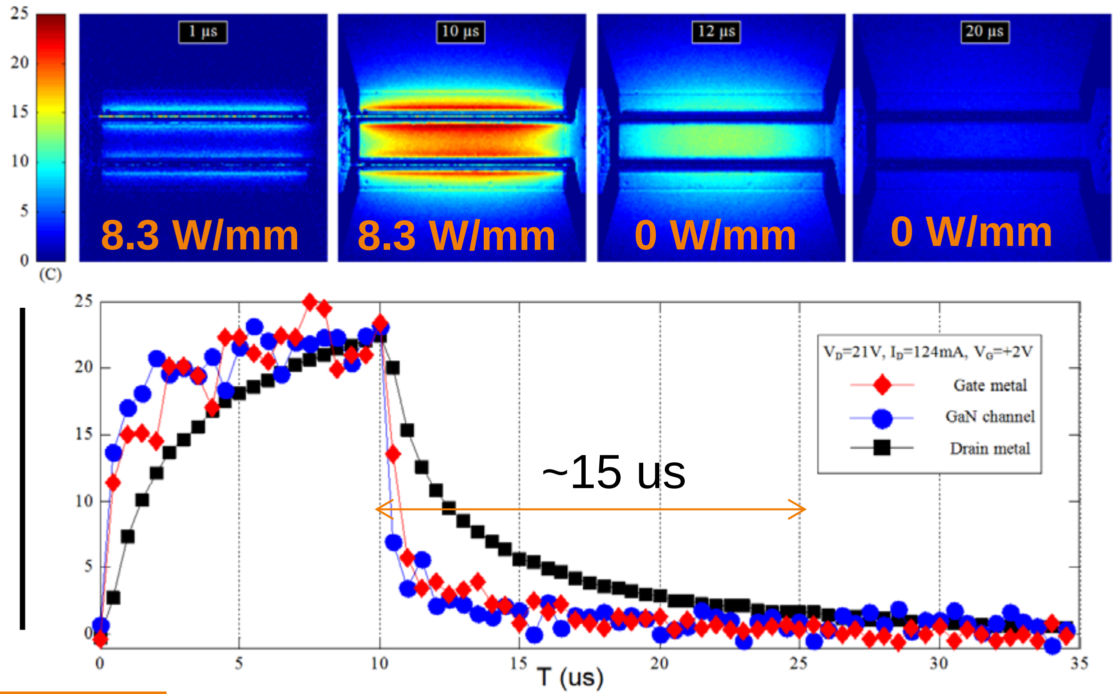
Physics of Failure (PoF) Enabler

3. Ratio of Power Density to Volumetric Heat Capacity:

- **Example: About 10x greater for GaN vs GaAs.**
- **Concern: Faster T transients. GaN heat capacity ($J/cm^3/K$) only a little greater.**
- ***But, with application specific awareness*, does not look like a problem.**

~15 us





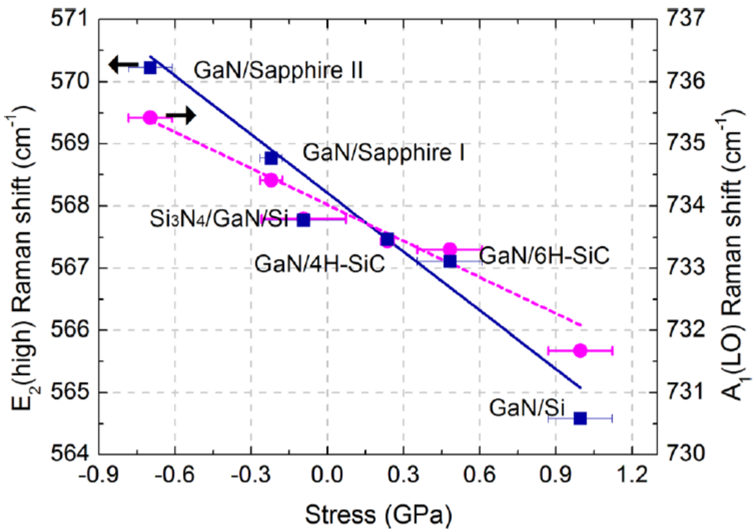
Possible Mitigation Options:
- **Measure or de-rate to address fast transients.**

K. Maize, E. Heller, D. Dorsey, A. Shakouri, "Fast Transient Thermoreflectance CCD Imaging of Pulsed Self Heating in AlGaN/GaN Power Transistors", 2013 IRPS Session 3C: Compound/Opto Electronics

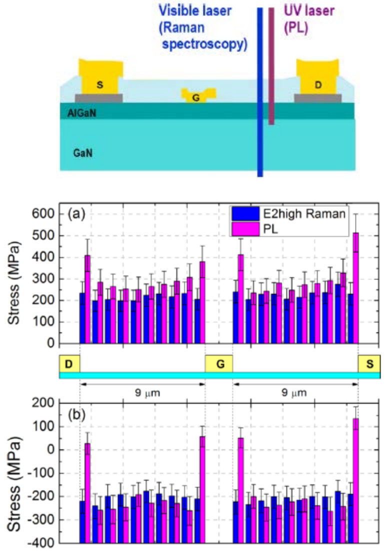
Physics of Failure (PoF) Enabler

5b. Substrate Coeff. of Thermal Expansion (CTE) mismatch

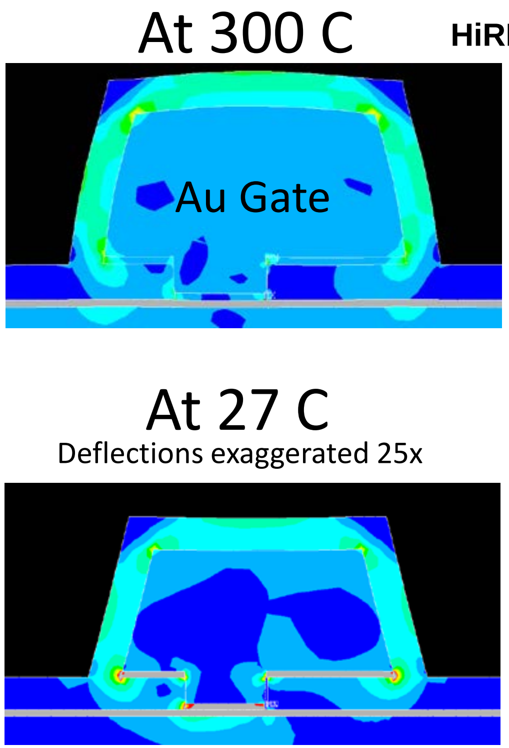
– **Big Si/SiC/Sapphire differences. Diamond?**



Sukwon Choi, Eric Heller, Donald Dorsey, Ramakrishna Vetury, and Samuel Graham, "Analysis of the residual stress distribution in AlGaN/GaN high electron mobility transistors", J. Appl. Phys. 113, 093510 (2013).].



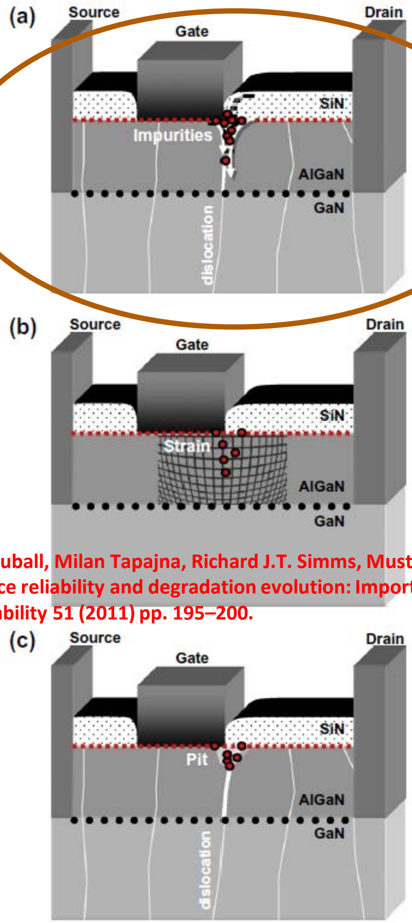
HiREV



Possible Mitigation Options:

- **GaN HEMTs appear robust to normal cycling.**
- **Test and/or Limit on/off thermal cycling at extremes of storage and use cases. Include power cycling in testing.**

PoF-E: High Dislocation Density



Low E_a Diffusion?!

"showed thermal activation energies of **~0.26 eV** consistent with diffusion processes along dislocations, with possible additional contributions from bulk diffusion accelerated by converse/inverse piezo-electric strain and leakage currents."

M. Kuball, Milan Tapajna, Richard J.T. Simms, Mustapha Faqir, and Umesh K. Mishra, "AlGaN/GaN HEMT device reliability and degradation evolution: Importance of diffusion processes" Microelectronics Reliability 51 (2011) pp. 195–200.

GaN laser diode "thermal Activation Energy has been extrapolated to be equal to **250 meV**"

Nicola Trivellin, Matteo Meneghini, Gaudenzio Meneghesso, Enrico Zanoni, Kenji Orita, Masaaki Yuri, Tsuyoshi Tanaka, and Daisuke Ueda, "Reliability analysis of InGaN Blu-Ray **laser diode**", Microelectronics Reliability 49 (2009) 1236–1239.

Fail mode often sqrt(time)
→ diffusion blamed again

Dislocations?
Not in active region
but in other places!

Possible Mitigation Options:

- **Long term testing. As long as possible. ALT for 10,000 hours has been done.**
- **Beware process changes increasing dislocation density, adding more oxygen or other impurities.**
- **Limit Vd and Vg; Select for lowest initial Ig leakage devices. Expect high dependence on process.**